IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket: NL 000133
NATALINO GIORGIO BUSA ET AL.	Examiner: DANIEL H. PAN
Serial No. 09/801,080	Group Art Unit: 2183
Filed: MARCH 7, 2001	Confirmation No. 5082

Title: DATA PROCESSING DEVICE, METHOD OF OPERATING A DATA PROCESSING DEVICE AND METHOD FOR COMPILING A PROGRAM

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CORRECTED APPEAL BRIEF

Sir:

Appellants herewith respectfully present a corrected **Summary of the Claimed Subject Matter** and a corrected **Grounds of Rejection to Be Reviewed on Appeal** of the Brief on Appeal, responsive to the Notice of Non-Compliant Appeal Brief mailed on March 3, 2008, related to a Brief on Appeal that was submitted on July 27, 2006.

Regarding Summary of the Claimed Subject Matter

Please delete the originally submitted "Summary of the Claimed Subject Matter" submitted in the Appeal submitted for consideration on December 6, 2006 and the "Corrected Summary of the Claimed Subject Matter" submitted for consideration on May 21, 2007 and substitute the "Summary of the Claimed Subject Matter" included herein.

Regarding Summary of the Claimed Subject Matter

Please delete the originally submitted "Grounds of Rejection to Be Reviewed on Appeal" submitted in the Appeal submitted for consideration on December 6, 2006 and the "Corrected Grounds of Rejection to Be Reviewed on Appeal" submitted for consideration on May 21, 2007 and substitute the "Grounds of Rejection to Be Reviewed on Appeal" included herein.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present system, for example as claimed in claim 1, relates to a data processing device (e.g., see, FIG. 1 and the accompanying description on page 5, lines 10-11) including a master controller (1); a first functional unit (2) including a slave controller (20); a second functional unit (3); and a common memory (11) shared by the first and second functional units (e.g., see, page 5, lines 10-13). The data processing device is programmed to execute an instruction by the first functional unit involving input/output operations by the first functional unit (e.g., see, page 5, lines 14-16). Execution by the data processing device involves at least one of: output data of the first functional unit being processed by the second functional unit during execution of the instruction (e.g., see, page 5, lines 16-17), and the input data to the first functional unit being generated by the second functional unit during execution of the instruction (e.g., see, page 5, lines 17-18).

The present method, for example as claimed in claim 4, relates to a method of operating a data processing device (e.g., see, FIG. 1 and the accompanying description on page 5, lines 10-11) including a master controller (1) for controlling operation of the data processing device (see, page 4, line 3), a first functional unit (2), which includes a slave controller (20), the first functional unit being arranged for executing instructions of a first type corresponding to operations having a relatively long latency (see, page 5, lines 20-22), a second functional unit (3) capable of executing instructions of a second type corresponding to operations having a relatively short latency (see, page 5, lines 22-24). The first functional unit (2), during execution of an instruction of the first type receives input data and provides output data (see, page 5, lines 14-6). Execution involves at least one of: output data of the first functional unit (2) being processed by the second functional (3) unit during execution of the instruction (see, page 5, lines 16-17), and input data to the first functional unit (2) being generated by the second functional unit (3) during execution of the instruction (see, page 5, lines 17-18).

An example of such a device and method is provided more particularly in the present specification in FIGs. 5 and 6B and the accompanying description at page 10, line 27, to page 11, line 19. In Figure 6b, inputs are not presented simultaneously, nor are outputs presented simultaneously. The input i1 (= p + q) is presented to the complex functional unit as soon as it is available, in cycle 1. During cycles 1 and 2, the second input i2 (= p - q - 2) is prepared and is then presented to the complex functional unit in cycle 3. Also in cycle 3, the first output o1 (= 2*i2 + 3) is presented. During cycles 3, 4 and 5, the output o2 (= 5*i1 + 2*i2 + 1) is computed and presented. During cycles 4 and 5, o1 (previously made available in cycle 3) is squared and the value 100 is subtracted to form a partial result as part of the condition checking in the last statement of Figure 5. In cycles 6 and 7, o1 is squared and the resulting quantity added to the partial result. Finally, in cycle 8, the inequality is evaluated.

In this example, it may be seen that output data (e.g., o1) of the complex functional unit ("first functional unit") is processed by the other functional unit ("second functional unit") during

execution of the instruction (e.g., 2Dtransform) by the complex functional unit ("first functional unit") as recited in claim 4. Also, input data (e.g., i2) to the first functional unit is generated by the second functional unit during execution of the instruction as recited in claim 4.

It should be explicitly noted that it is not the Appellants' intention that the currently claimed device and method be limited to operation within this illustrative device and method beyond what is required by the claim language. Description of the illustrative device and method is provided indicating portions of the claims which cover the illustrative device and method merely for compliance with requirements of this appeal without intending any further interpreted limitations be read into the claims as presented.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-5 of U.S. Patent Application Serial No. 09/801,080 are anticipated under 35 U.S.C. §102(b) over U.S. Patent No. 4,876,643 to McNeill ("NcNeill") and whether claim 5 of U.S. Patent Application Serial No. 09/801,080 is anticipated under 35 U.S.C. §102(e) over U.S. Patent No. 6,266,766 to O'Connor ("O'Connor"). The Appellants respectfully wish the Board to address the patentability of independent Claims 1 and 4, and further Claims 2, 3, and 5, as depending on one of Claims 1 and 4, based on the requirements of Claims 1 and 4. This position is provided for the specific and stated purpose of simplifying the current issue on appeal. However, the Appellants herein specifically wish to reserve the right to argue and address the patentability of each of the further claims at a later date should the separately patentable subject matter of those claims later become an issue. Accordingly, this limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of Claims 1 and 4, is not intended

as a waiver of Appellants' right to argue the patentability of the further claims and claim elements at that later time.

CONCLUSION

In view of the above, it is respectfully submitted that the Brief on Appeal is compliant and consideration on the merits is respectfully requested.

Respectfully submitted,

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March 7, 2008

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